IN THE CLAIMS

Please amend claims 1, 3 through 5, 7, 9, and 10, to read as follows:

·ī-	1 (amended twice). A flat panel display apparatus for receiving display
2	information including video data and synchronizing data from a host processing digital
3	data in a serial digital communication, said display apparatus adapted for operation
4	without need for any — (i) analog-to-digital converter (ADC) or (ii) phase-locked loop
5	(PLL) circuit — for signal conversion, said display apparatus comprising:
6	a receiver for reconstructing said display information;
7	a synchronizing signal generator for generating a synchronizing signal by
8	extracting the synchronizing data from said reconstructed display
9	information;
10	a digital-to-analog converter (DAC) for converting said video data to a
11	corresponding analog video signal; and
12	an output terminal for externally transferring said synchronizing signal and
13	analog video signal to an analog display apparatus.

3 (amended twice). A digital data processing system including a host computer for processing digital data and a flat panel display apparatus for displaying display

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3	information received from said host computer, said system comprising:
4	a transmitter connected to said host to transfer digital display information as
5	serial data;
6	a receiver for reconstructing said digital display information;
7	a synchronizing signal generator for generating a synchronizing signal by
8	extracting synchronizing data from said reconstructed display
9	information;
10	a digital-to-analog converter (DAC) for converting video data to a
11	corresponding analog video signal; and
12	an output terminal for externally transferring said synchronizing signal and
13	said analog video signal to an analog display apparatus;
14	wherein said flat panel display apparatus includes said receiver, said synchronizing signal
15	generator, and said output terminal; and
16	wherein said flat panel display apparatus does not utilize any — (i) analog-to-digital
17	converter (ADC) or (ii) phase-locked loop (PLL) circuit — for signal conversion.
1	4 (amended twice). The display apparatus of claim 2, further comprising:
2	a liquid crystal display (LCD) driver for receiving data output from said
3	video data converter; and

an LCD display panel for receiving an output from said LCD driver.

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1	5 (amended thrice). The display apparatus of claim 1, said analog display
2	apparatus comprising:
3	an amplifier for receiving said video signal from said DAC via said output
4	terminal and amplifying said video signal;
5	a deflection signal generator for receiving said synchronizing signal output
6	from said synchronizing signal generator via said output terminal and
7	for generating deflection signals;
8	a high voltage generator for receiving an output from said deflection signal
9	generator and generating a high voltage; and
10	a cathode ray tube (CRT) display for receiving said amplified video signal
11	from said amplifier and output signals from said deflection signal
12	generator and a high voltage from said high voltage generator.
1	7 (amended twice). The system of claim 6, further comprising:
2	a liquid crystal display (LCD) driver for receiving data output from said
3	video data converter; and
4	an LCD display panel for receiving an output from said LCD driver.

1	9 (amended). In a flat panel display apparatus comprising:
2	a receiver means for reconstructing video display information including
3	video synchronization data from a host; and
4	a conversion means for converting said data to a corresponding video
5	signal;
5	the improvement comprising:
7	a means for converting said data to a corresponding video signal without
3	utilization of (i) an analog-to-digital converter (ADC) or (ii) a phase-locked
9	loop (PLL) circuit.
1	10 (amended). In a method of processing display information containing video
2	data and synchronizing data from a host processing digital data in a serial communication,
3	said method comprising the steps of:
4	(1) reconstructing said display information to provide reconstructed display
5	information;
6	(2) generating a synchronizing signal by extracting the synchronizing data from
7	said reconstructed display information;
8	(3) converting said video data to a corresponding video signal; and

9	(4) transferring said synchronizing signal and video signal to a display;
10	the improvement comprising: a step for converting said video data to a corresponding
11	signal without utilizing (i) an analog-to-digital converter (ADC) or (ii) a phase-
12	locked loop (PLL) circuit.